**Homework 7**

Trevor Lund, CprE 381

1. Tracing Pipelined MIPS Code
   1. $5 = 62, $6 = 45, $8 = 16, $7 = 23, $9 = 1  
      Cycle # : IF/ID register; ID/EX; EX/MEM; MEM/WB  
      Cycle 1 : lw instruction, NULL, NULL, NULL  
      Cycle 2 : add instruction; 25, 22; NULL; NULL  
      Cycle 3 : and instruction; 23, 22; 62; NULL  
      Cycle 4 : or instruction; 24, 23; 45; 1062  
      Cycle 5 : sub instruction; data1 = 22, data2 = 21, rs = 7, rt = 2, rd = 1; ALU = 16, port2 = 23, rd/rt = 3; dmem = 1045, ALU = 45, rd = 2
   2. $2 = 44, $4 = -2, $5 = 50, $7 = 47, $8 = 48  
      Cycle 1 : add2; NULL; NULL; NULL  
      Cycle 2 : sub4; add2; NULL; NULL  
      Cycle 3 : add5; sub4; add2; NULL  
      Cycle 4 : add7; add5; sub4; add2  
      Cycle 5 : add8; add7; add5; sub4  
        
      In cycle 5, registers $2 and $6 will be read from, and $8 will be written to.
2. Data Hazards and Forwarding
   1. RAR: $2(1 and 4)(1 and 3)(3 and 4)(1 and 2)(2 and 3)(2 and 4)  
      $1(2 and 4)  
      WAW: $1(1 and 3)  
      RAW: $1(1 and 4)(3 and 4)(1 and 2)  
      WAR: $2(1 and 4)(2 and 4)(3 and 4)  
      $1(2 and 3)  
        
      Data Hazards to forward:  
      RAW: $1(1 and 2)  
      Data Hazards to stall:  
      RAW: $1(3 and 4)  
      WAR: $1(2 and 3), $2(3 and 4)